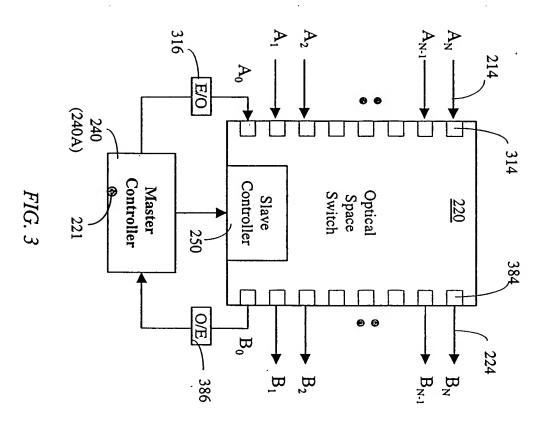
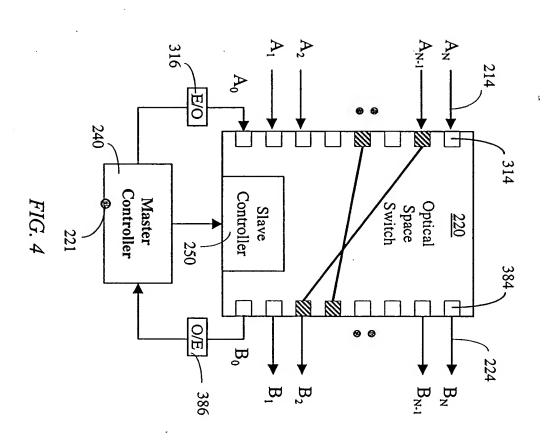


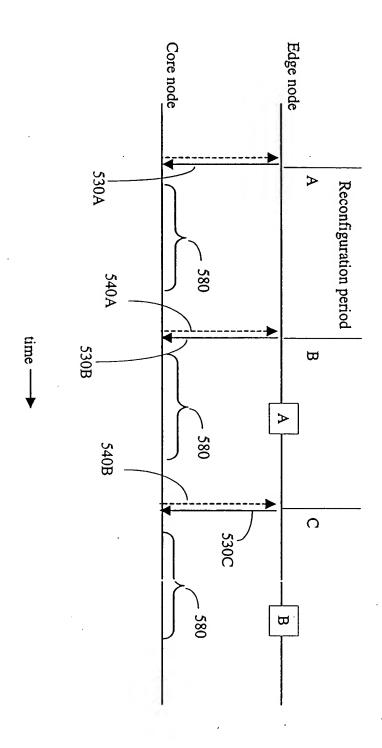
FIG. 2





Channel switched

Burst switches



71G. 5

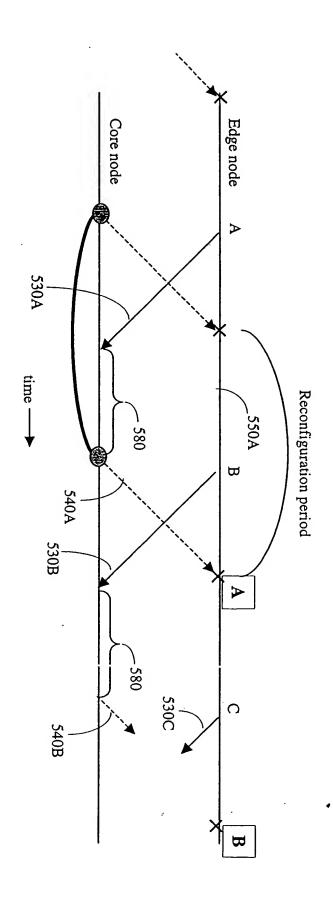


FIG. 6

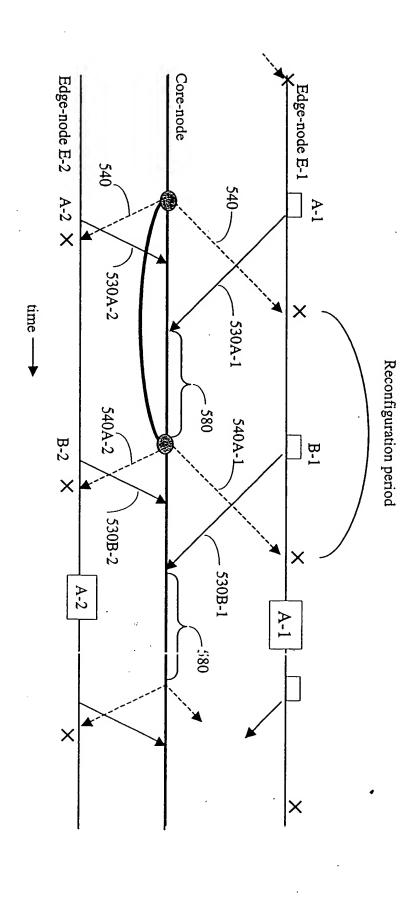
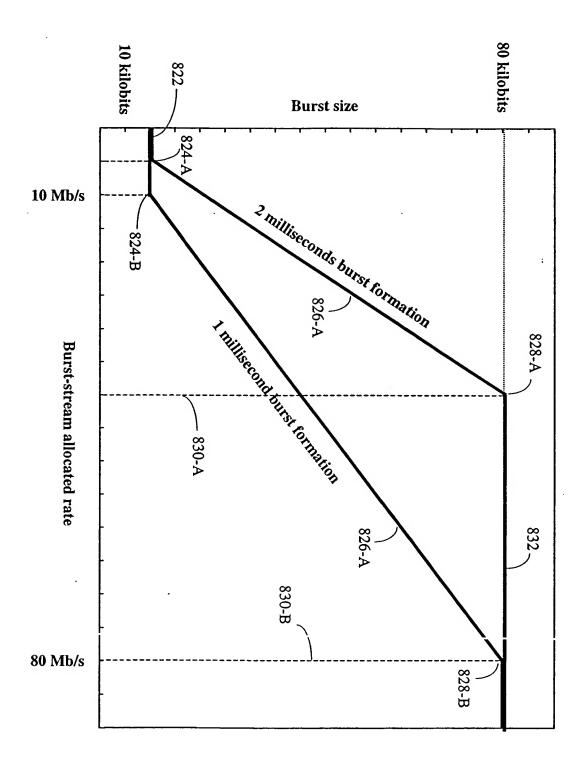
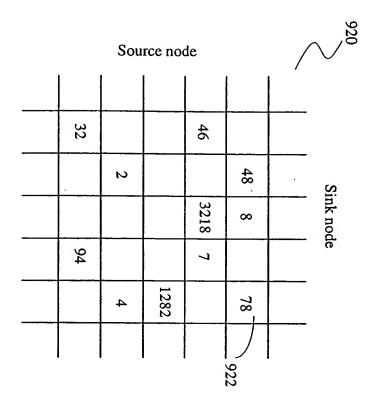
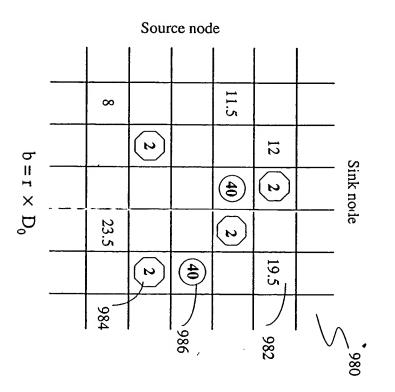


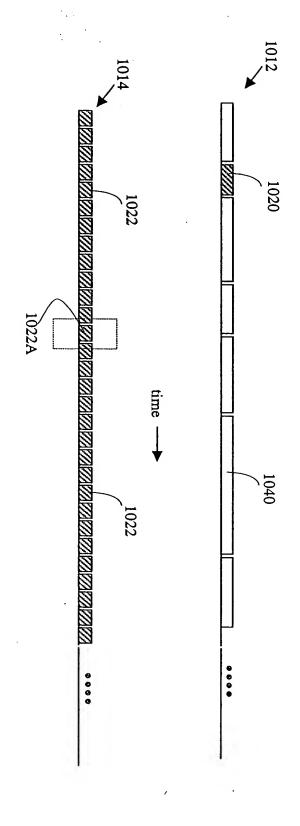
FIG. 7

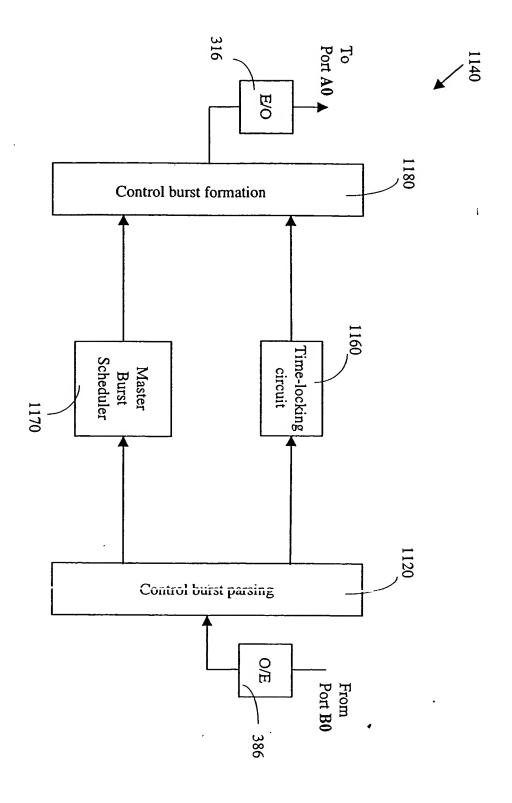


71G. 8









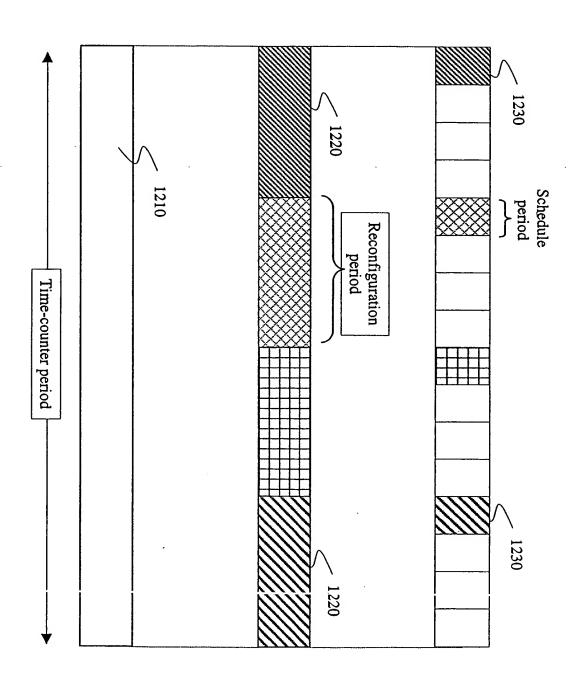
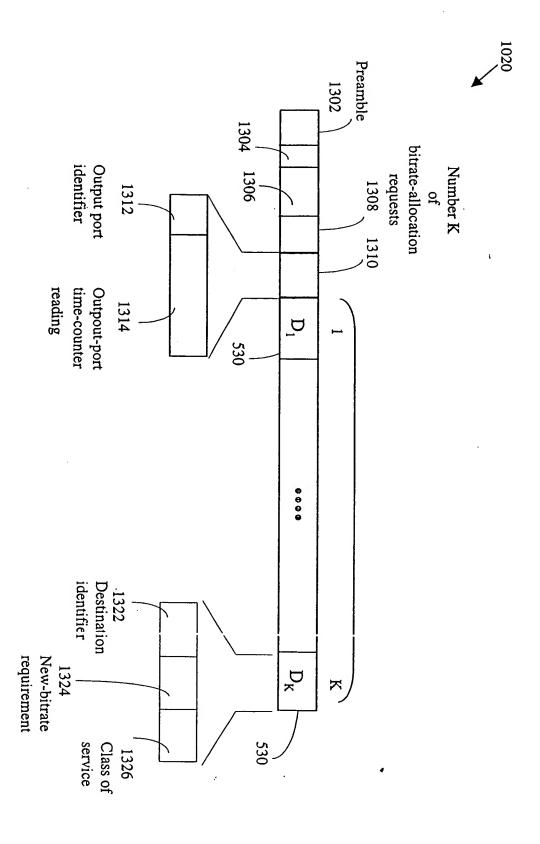


FIG. 12



j

FIG. 13

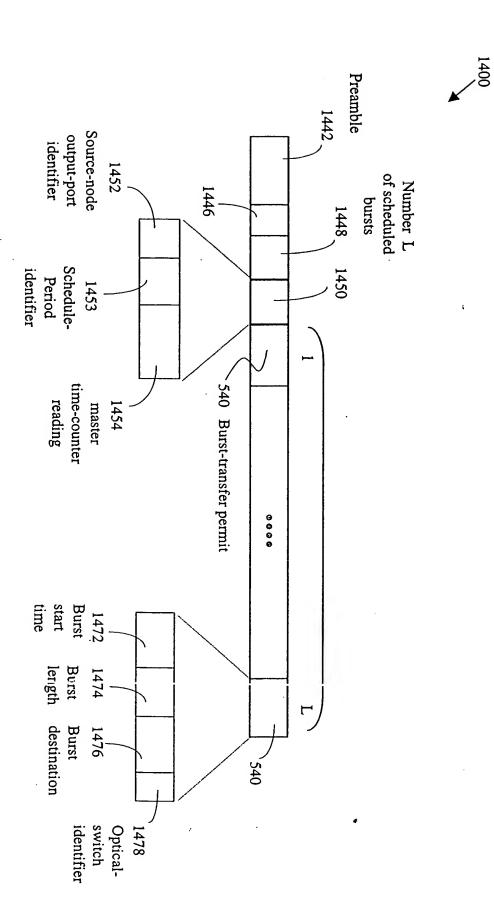
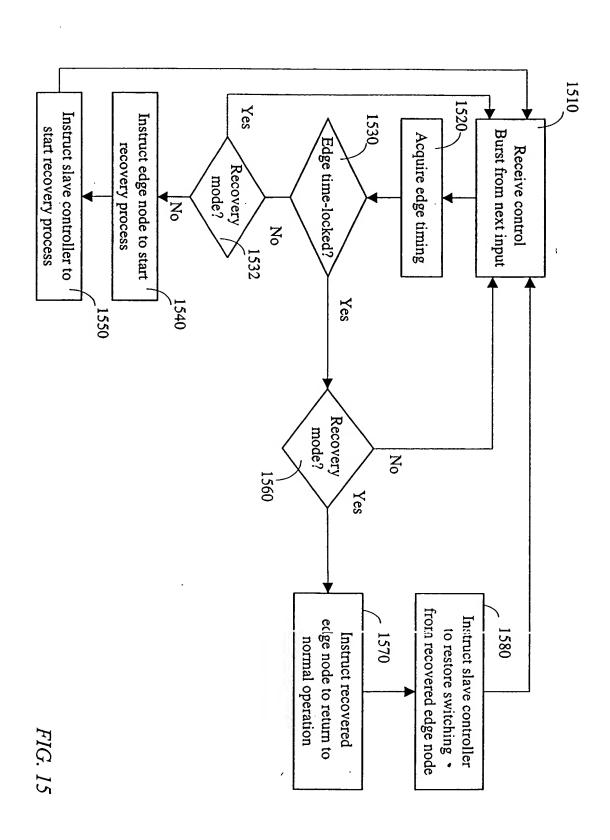


FIG. 14



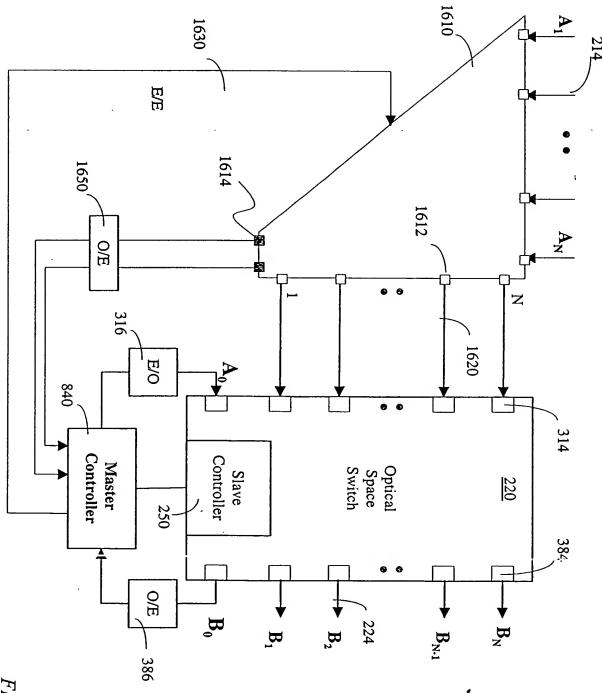
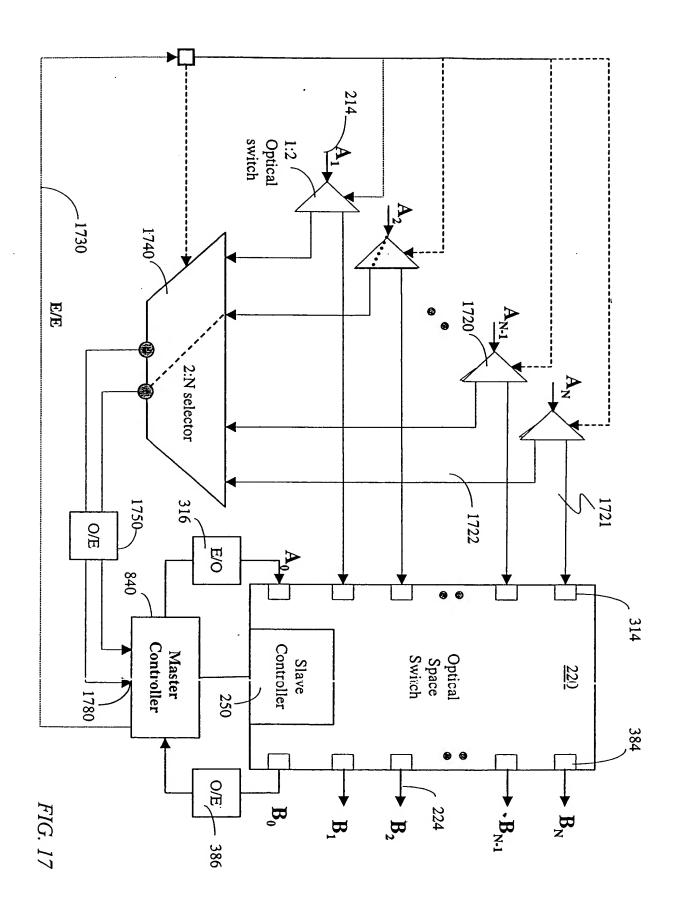
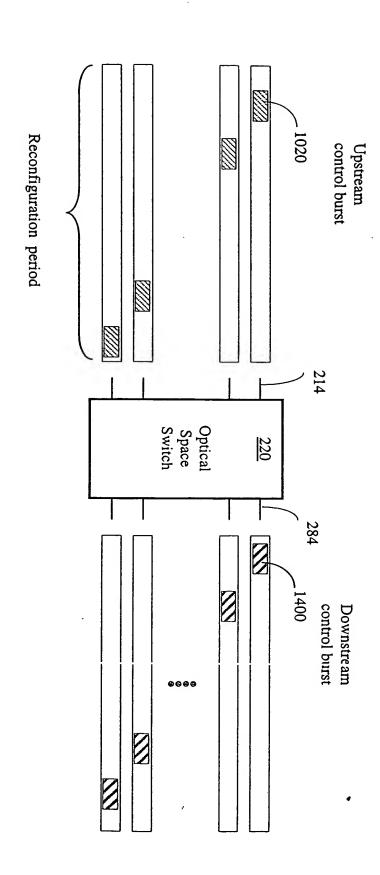


FIG. 16





Time-counter cycle (master cycle) Period: 2^w time slots

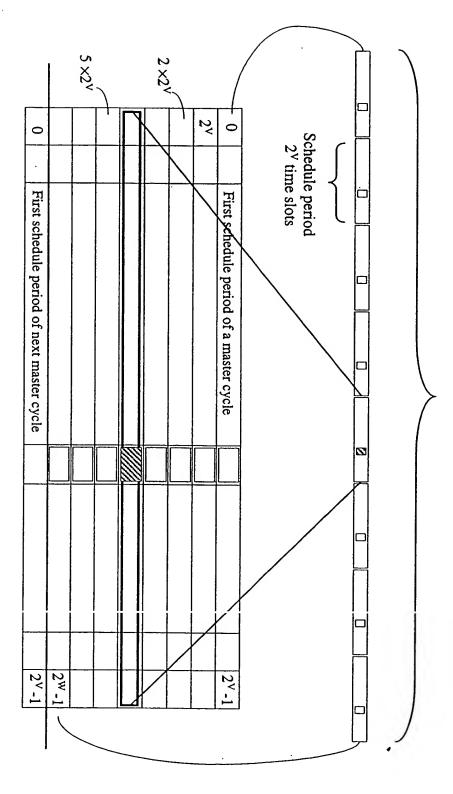
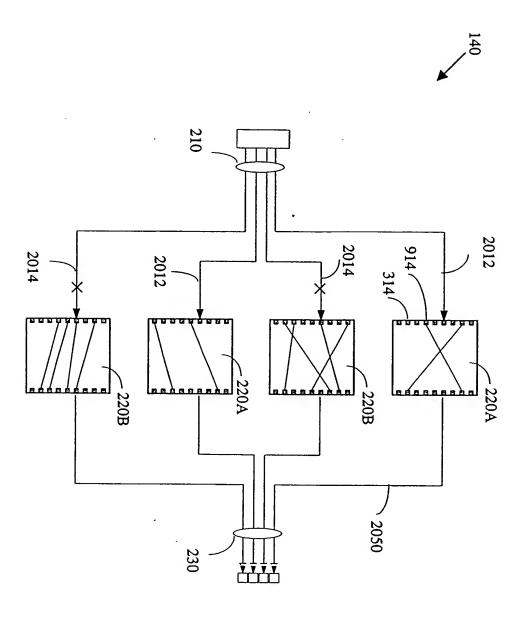


FIG. 19



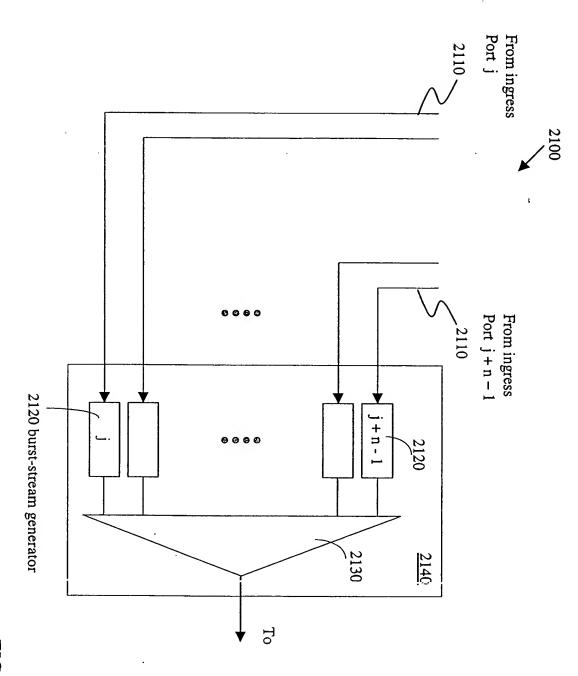


FIG. 21

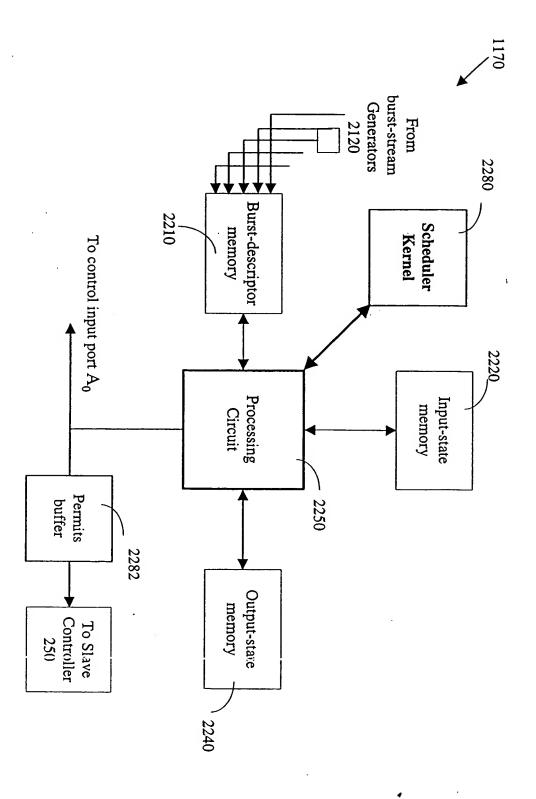


FIG. 22

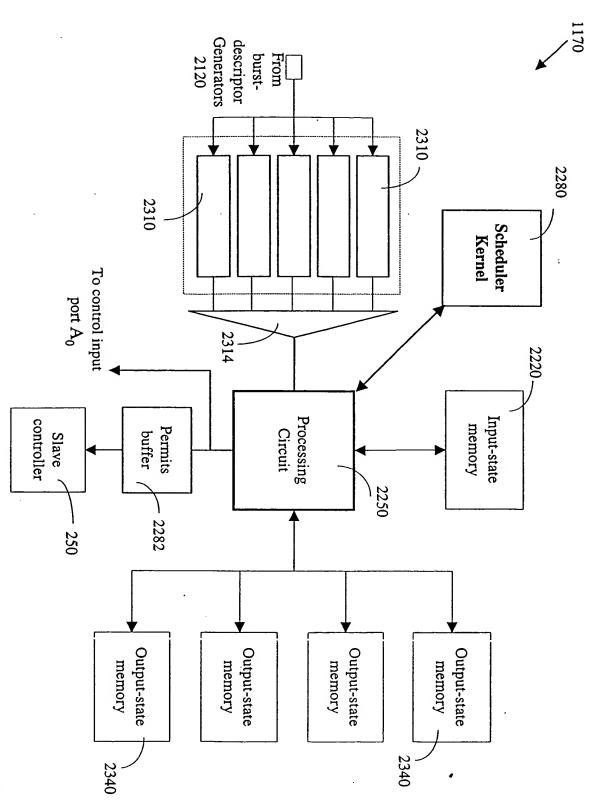
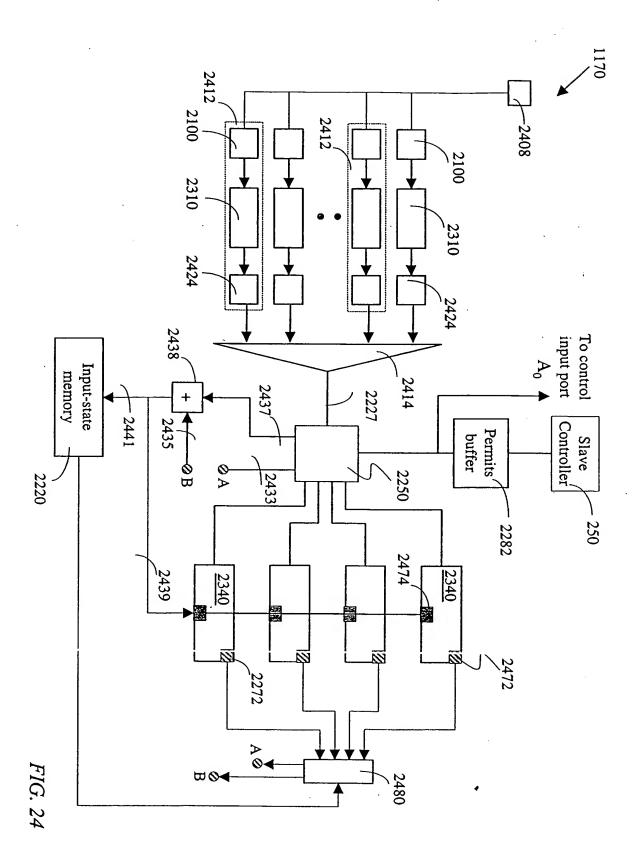


FIG. 23



J

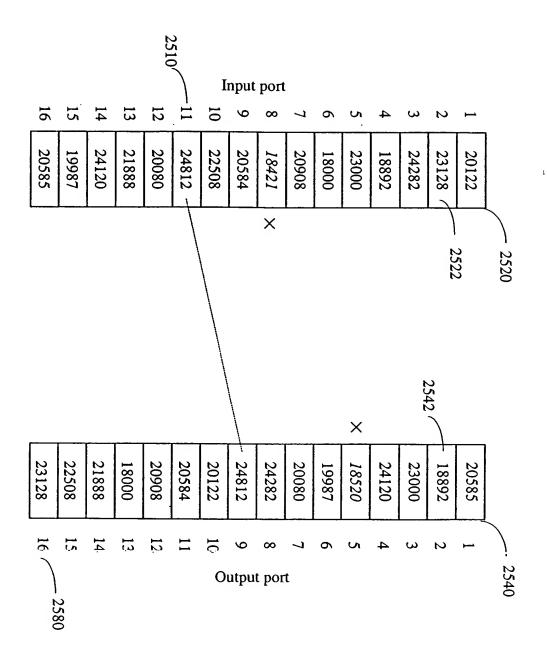


FIG. 25

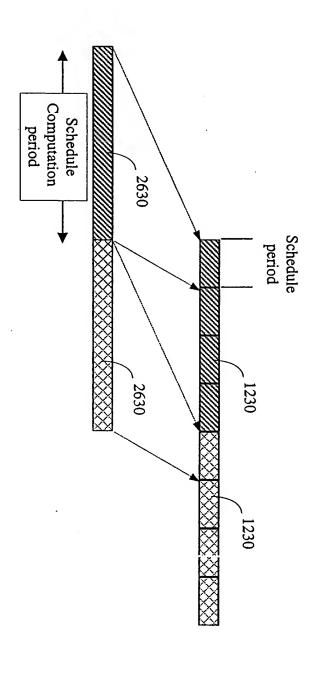
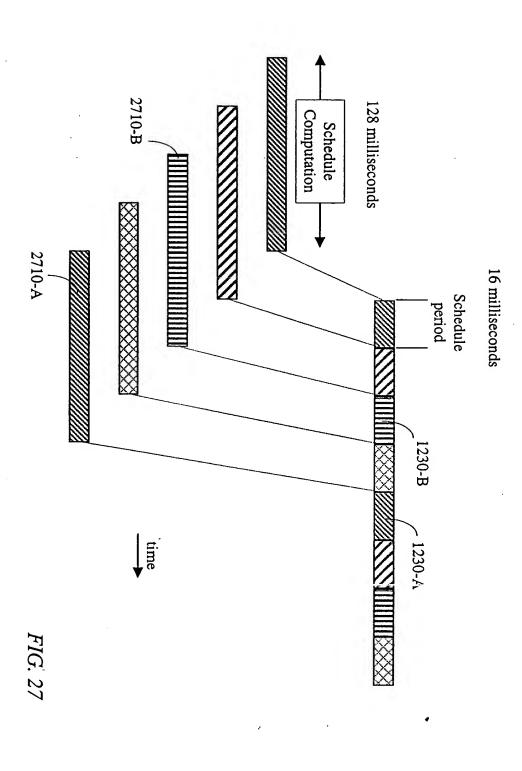
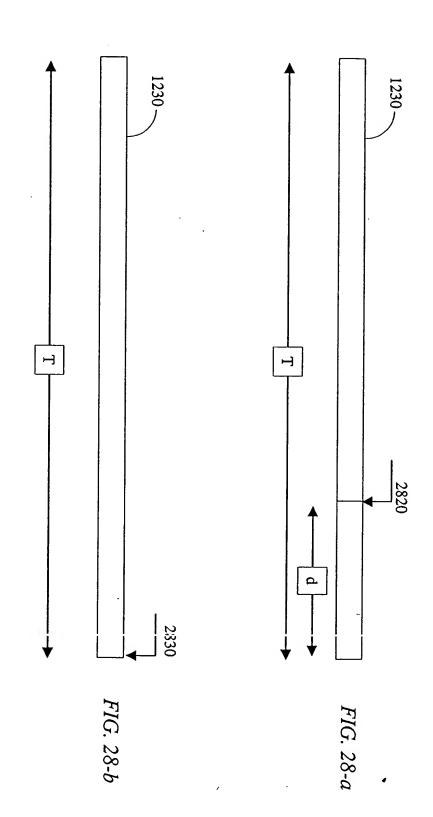


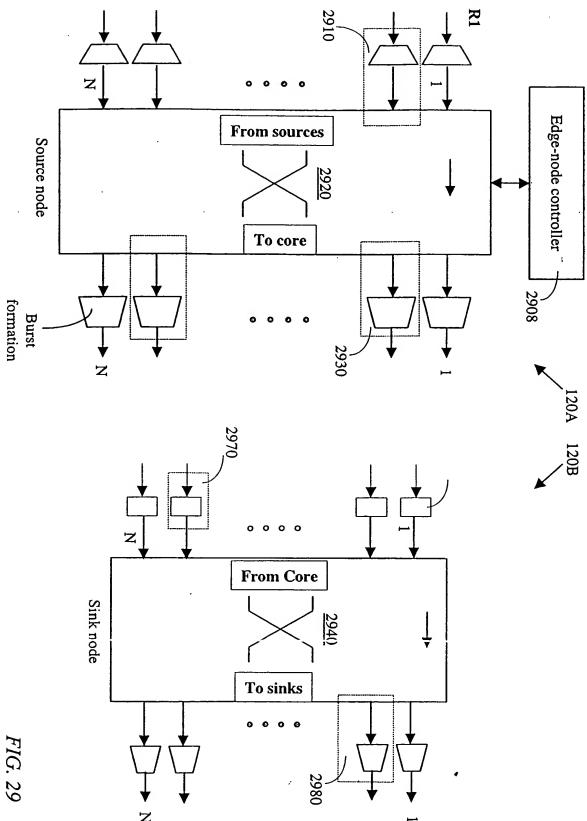
FIG. 26





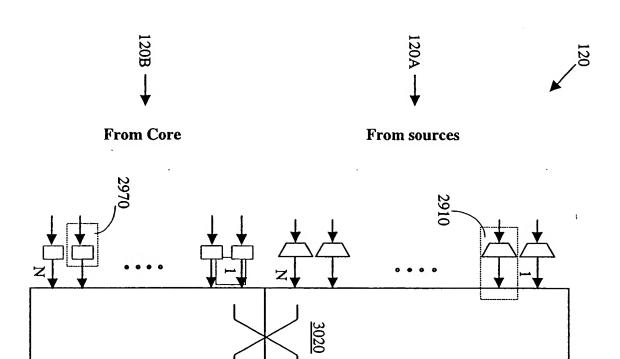
j

FIG. 28



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- }





To core

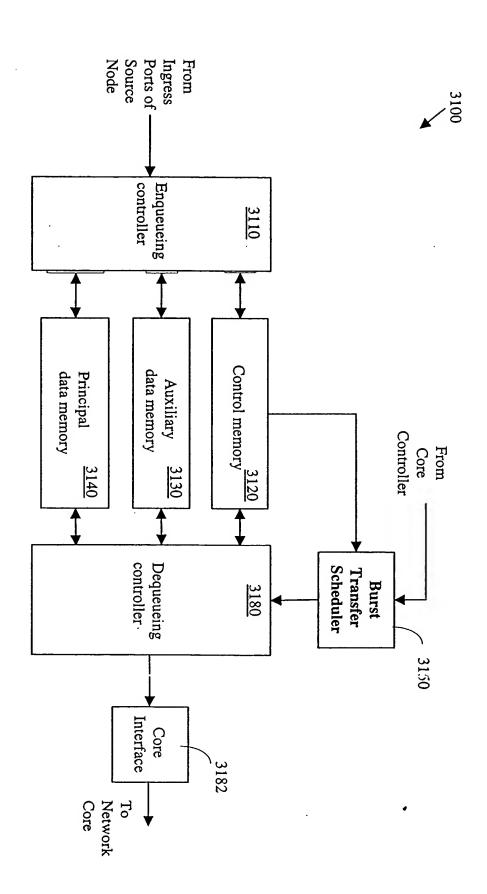


FIG. 31

-i,

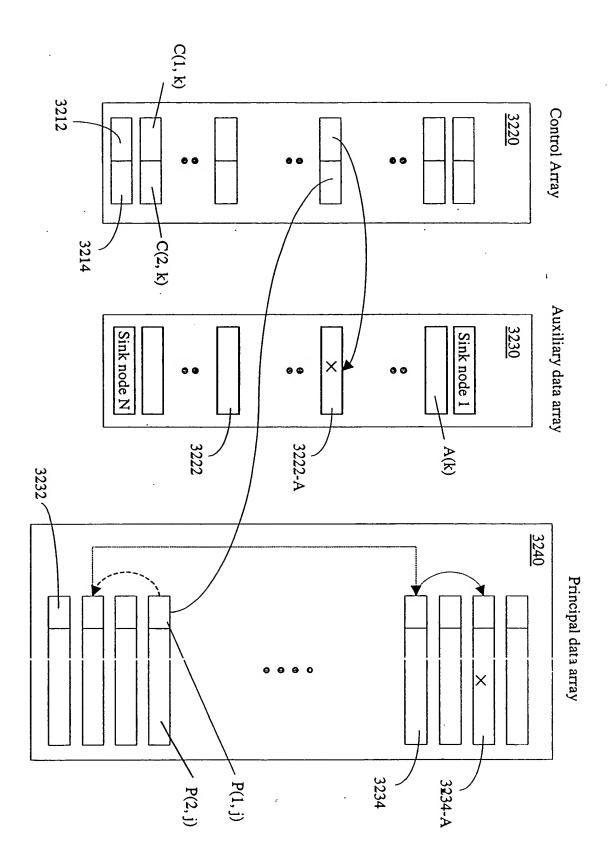


FIG. 32

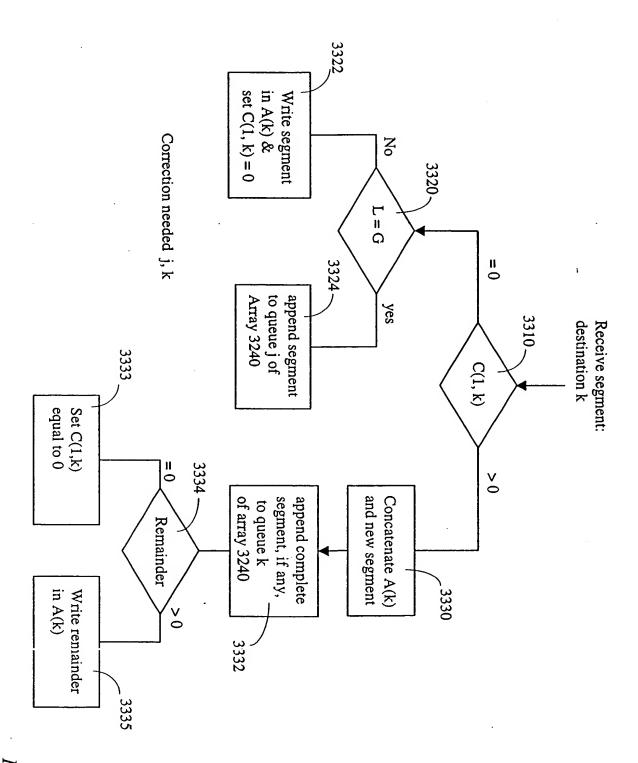


FIG. 33

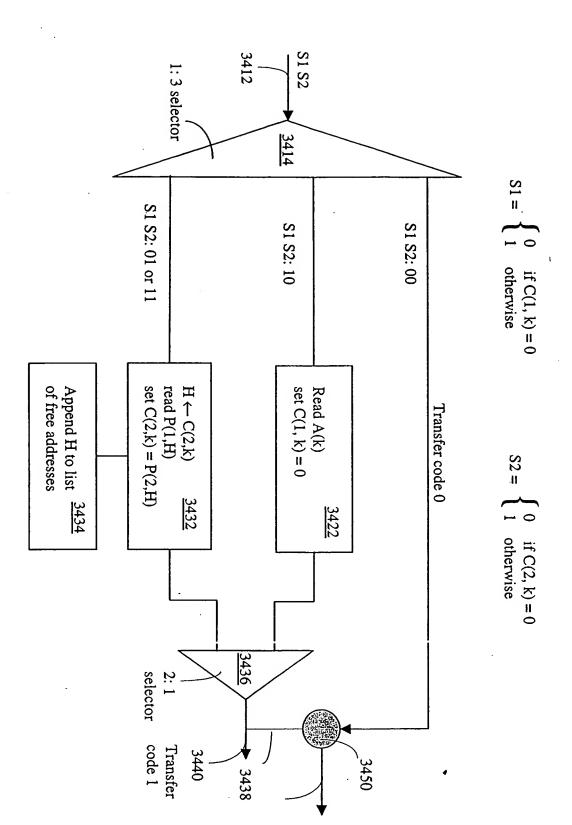


FIG. 34